GaAs Monolithic MIC's for Direct Broadcast Satellite Receivers

SHIGEKAZU HORI, MEMBER, IEEE, KIYOHO KAMEI, KIYOYASU SHIBATA, MIKIO TATEMATSU, KATSUHIKO MISHIMA, AND SUSUMU OKANO

Abstract—**A 12-GHz low-noise amplifier (LNA), a 1-GHz IF amplifier (IFA), and an 11-GHz dielectric resonator oscillator (DRO) have been developed for DBS home receiver applications by using GaAs monolithic microwave integrated circuit (MMIC) technology. Each MMIC chip contains FET's as active elements and self-biasing source resistors and bypass capacitors for a single power supply operation. It also contains dc-block and RF-bypass capacitors.**

The three-stage LNA exhibits a 3.4-dB noise figure and a 19.5-dB gain over 11.7–12.2 GHz. The negative-feedback-type three-stage IFA shows a 3.9-dB noise figure and a 23-dB gain over 0.5–1.5 GHz. The DRO gives 10-mW output power at 10.67 GHz, with a frequency stability of 1.5 MHz over a temperature range from −40–80 °C. A direct broadcast satellite (DBS) receiver incorporating these MMIC's exhibits an overall noise figure of ≤ 4.0 dB for frequencies from 11.7–12.2 GHz.

I. Introduction

TELEVISION BROADCAST SYSTEMS via 12-GHz direct broadcast satellites (DBS) are scheduled to enter into operation in various countries in the mid 1980's. Success of such systems, however, depends heavily on the availability of low-noise 12-GHz receivers in large quantities at an acceptable price. In view of the potential of large-scale production and low cost, the GaAs monolithic microwave integrated circuit (MMIC) seems to be the most viable candidate for the receiver application.

Extensive efforts are being directed in various laboratories toward the development of GaAs MMIC's for application to outdoor units of DBS receivers [1]–[3]. As shown in Fig. 1, a typical outdoor unit is composed of a GaAs FET low-noise amplifier (LNA), a bandpass filter, a mixer, an IF amplifier (IFA), and a dielectric resonator oscillator (DRO). This paper describes three kinds of FET-based GaAs MMIC's (LNA, IFA, and DRO) that have been developed for actual operation in an experimental outdoor unit. Each MMIC chip has been designed to operate under a single power supply by incorporating self-biasing resistors and capacitors and to have dc-block and RF-bypass capacitors.

The LNA and IFA chips are mounted in ceramic packages for easy handling, and the DRO chip is mounted in a hermetically sealed housing, together with a dielectric resonator, to avoid a moisture effect. The FET's and resistors in the IFA and DRO chips are fabricated by selective direct ion implantation into a semi-insulating GaAs substrate. These MMIC's have been successfully employed in the outdoor unit of a DBS home receiver. The following sections describe circuit design, fabrication, packaging, and RF performance of the MMIC's.

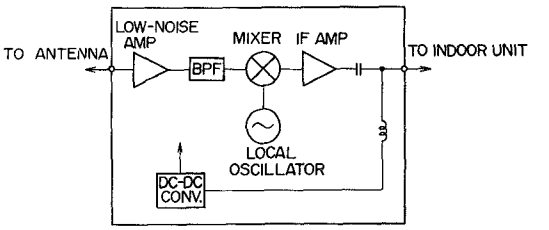

Fig. 1. Typical block diagram of an outdoor unit of a DBS receiver.

II. Circuit Design

A. Low-Noise Amplifier

The design goal was to build a low-noise amplifier with a noise figure of ≤ 3.5 dB and a gain of ≥ 20 dB at 12 GHz. In order to fulfill this goal, a three-stage FET amplifier was chosen. Prior to the three-stage design, however, a single-stage amplifier was built and thoroughly tested.

Figs. 2 and 3 show the circuit diagram and the top view of the single-stage LNA chip, respectively. The chip measures 1.5×1.5 mm. The noise figure of an FET usually improves with decreasing gate length, as previously demonstrated by some authors with a quarter-micrometer gate GaAs FET fabricated using electron-beam lithography [4]. In the present work, however, the FET gate length was chosen to be 0.4 μm by making tradeoffs between noise figure and device yield in the future production phase. The gate is also designed to have a width of 200 μm and a single pad to minimize the gate–source overlay parasitic capacitance. The source electrodes outside the FET are tapered to reduce the source inductance.

In order to obtain the optimum source and load impedances for gain and noise figures of the FET, gain and noise parameters of a discrete FET equivalent to the FET to be employed in the MMIC were measured. Fig. 4 shows the constant noise figure (solid lines) and gain (dotted lines) circles for the source impedance at 12 GHz, where the inductance of 0.2 nH for the tapered grounding pattern is taken into account. It is found that the minimum noise figure of 1.9 dB and the associated gain of 7.5 dB are

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The authors are with the Microwave Solid-State Department, Electronics Equipment Division, Toshiba Corporation, 1 Komukai-Toshiba-cho, Saiwai-ku, Kawasaki 210, Japan.

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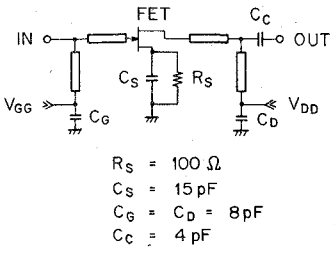

Fig. 2. Circuit diagram of a single-stage low-noise amplifier.

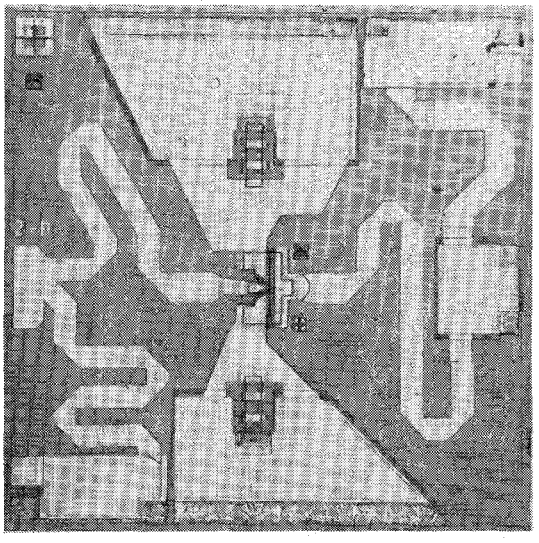

Fig. 3. Single-stage low-noise amplifier chip (1.5×1.5 mm).

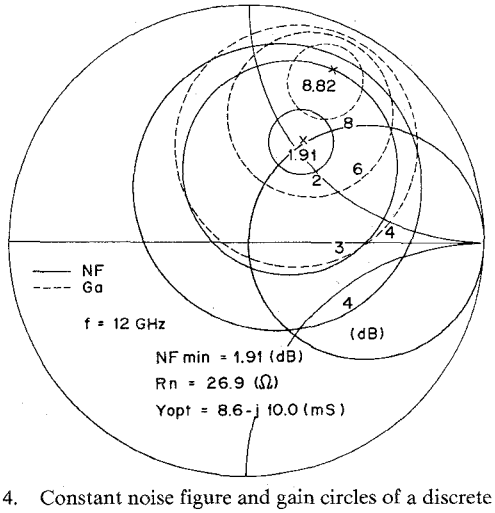

Fig. 4. Constant noise figure and gain circles of a discrete FET.

obtained for the optimum source admittance of $Y_{opt} = 8.6 - j10.0$ mS.

After the evaluation and analysis of the discrete FET, the input and output matching circuits of the single-stage LNA were designed to optimize a noise figure and realized by shunt- and series-connected microstrip lines with a characteristic impedance of 70 Ω. The shunt microstrip lines are terminated by RF-bypass capacitors. The length of each microstrip line is compensated by taking into account the effective line length reduction due to the coupling between lines [5]. The thickness of the GaAs

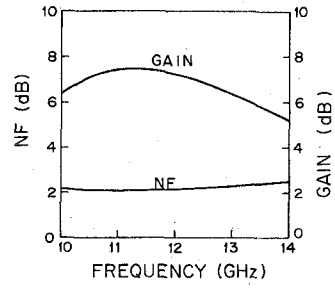

Fig. 5. Calculated noise figure and gain of a single-stage LNA as a function of frequency.

substrate has been chosen to be 300 μm by considering matching circuit loss, ease of chip handling, and less performance changes due to thickness variation.

The source resistor R_s and RF-bypass capacitor C_s are incorporated for single power supply operation. R_s is chosen to be 100 Ω to the drain current to 7 mA, at which the noise figure of the FET reaches a minimum. An external gate-bias terminal is also included in order to evaluate RF performance as a function of drain current. The capacitances of RF-bypass capacitors C_G and C_D, source capacitor C_s, and dc-block capacitor C_c are 8, 15, and 4 pF, respectively.

Fig. 5 shows the calculated RF performances of the single-stage LNA by taking into account the losses of microstrip lines and RF-bypass capacitors in the matching circuits. The minimum noise figure of 2.2 dB and the gain of 7.0 dB are predicted at 12 GHz.

After evaluation of the single-stage LNA, the three-stage LNA was designed. The circuit diagram and the top view of the three-stage chip with a size of 1.5×3.0 mm are shown in Figs. 6 and 7, respectively. The input and output matching networks of each stage have been optimized for a source and load impedance of 50 Ω. The input-matching circuits have been designed to optimize noise figure in the first and second stages and to optimize gain in the third stage. The source capacitor C_s and the resistor R_s are employed in every stage so that the LNA can be operated using a single power supply. The capacitors C_s, C_D, and C_c and the resistors R_s have the same values as the corresponding ones in the single-stage LNA. From the single-stage LNA performance, the RF performance of the three-stage LNA was predicted to have a minimum noise figure of 2.5 dB and a gain of 22 dB at 12 GHz.

B. IF Amplifier

The IFA has been designed to give a noise figure of ≤ 3.5 dB, a gain of ≥ 20 dB, and an input and output VSWR of ≤ 2.0 for frequencies from 0.5–1.5 GHz. Several approaches to amplifier designs in this frequency range have been proposed to date [6], [7]. However, most of them utilize a gate–drain resistive feedback around an individual FET with a relatively wide gate width. In order to reduce the gate width for lower dc power consumption, we have designed a three-stage monolithic IF amplifier in which the feedback resistor is connected between the input and output ports of the amplifier. The circuit diagram and the top

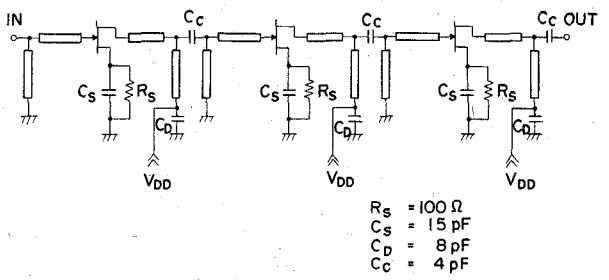

Fig. 6. Circuit diagram of a three-stage low-noise amplifier.

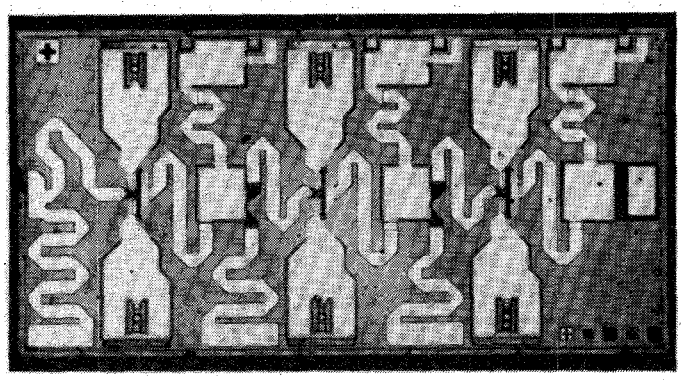

Fig. 7. Three-stage low-noise amplifier chip (1.5×3.0 mm).

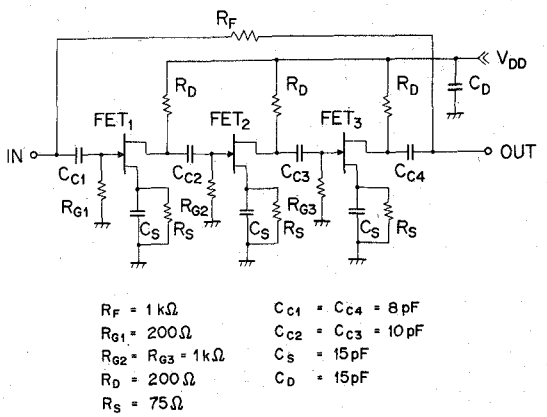

Fig. 8. Circuit diagram of a 1-GHz IF amplifier.

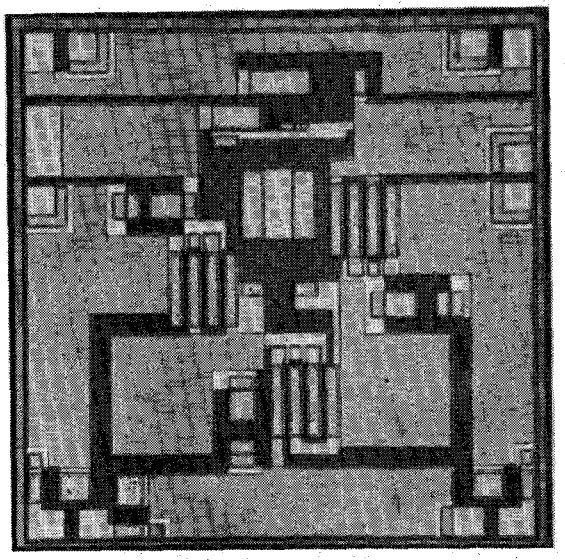

Fig. 9. IF amplifier chip (1.5×1.5 mm).

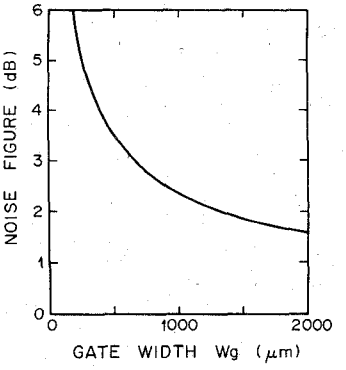

Fig. 10. Gate width dependence of an IFA noise figure.

view of the IFA chip with a size of 1.5×1.5 mm are shown in Figs. 8 and 9, respectively.

In the amplifier design, consideration was also given to ease of assembly and operation in DBS receivers. The source resistors R_s and bypass capacitors C_s are incorporated as in the LNA for single power supply operation. Furthermore, the drain resistors R_D and bypass capacitor C_D are connected to each drain and at the bias feed terminal, respectively. The drain resistors R_D together with the bypass capacitor C_D make it possible to eliminate the RF choke otherwise necessary outside the chip.

The gate of each FET has a length of 1 μm. Its width as well as the gate resistors R_{G1}, R_{G2}, R_{G3}, the drain resistors R_D, and feedback resistor R_F are optimized by a computer simulation in terms of gain flatness and input and output VSWR's. Fig. 10 shows the calculated noise figure as a function of the FET gate width [6]. The noise figure becomes lower as the gate width becomes wider. Its width is determined to be 600 μm by tradeoffs between noise figure and dc power consumption. The capacitor values are determined such that the performance does not degrade at the lowest frequencies of interest.

The predicted performance of the IFA shows a noise figure of $\leqslant 3.2$ dB, a gain of 22 ± 0.1 dB, and input and output VSWR's of $\leqslant 2.0$ at frequencies from 0.5–1.5 GHz.

C. Dielectric Resonator Oscillator

The local oscillator for DBS receiver applications is required to have a frequency stability of ± 1 MHz at a center frequency of 10.7 GHz over a temperature range of -40–$80\,^{\circ}$C. Among several types of MMIC oscillators proposed to date [8], [9], the dielectric resonator oscillator configuration is the most promising candidate for the local oscillator application in view of size and cost. We have designed a dielectric resonator oscillator which consists of an MMIC oscillator chip and a dielectric resonator circuit. The oscillator circuit diagram and the top view of the oscillator chip with a size of 1.5×1.5 mm are shown in Figs. 11 and 12, respectively.

Hybrid MIC technology is used to form the resonant circuit for frequency stabilization. The dielectric resonator is mounted on alumina substrate and coupled to a micro-

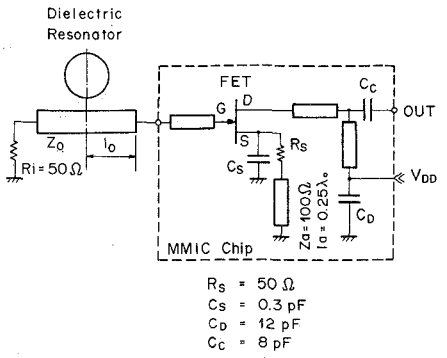

Fig. 11. Circuit diagram of a dielectric resonator oscillator.

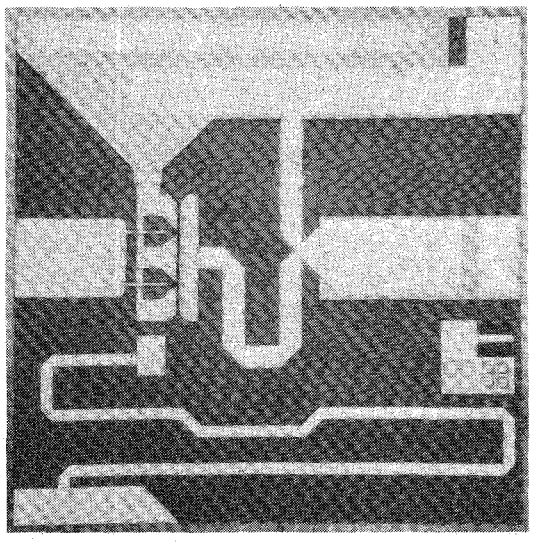

Fig. 12. Dielectric resonator oscillator chip (1.5×1.5 mm).

strip line terminated by a 50-Ω load. The dielectric resonator used has an unloaded Q of 7400, a relative dielectric constant of 36.3, and a resonant-frequency temperature coefficient of +6 ppm/°C.

The MMIC oscillator chip has a common-source configuration with a feedback capacitor C_s. An FET with a gate length of 1 μm and a width of 300 μm is used to obtain an oscillator output power of 10 dBm. The circuit design has been performed using the measured S-parameters of the equivalent discrete FET. The feedback capacitor C_s of 0.3 pF is determined by a computer simulation so as to make the output reflection coefficient at the drain terminal maximum under a given reflection coefficient of the resonant circuit with a loaded Q of 1000. The output matching circuit is optimized by a nonlinear analysis based upon the measured large signal impedance of the discrete FET [10]. It is composed of a series microstrip line and a shunt microstrip line terminated by the RF-bypass capacitor C_D.

The resistor R_s with a quarter-wavelength shunt stub was used for single power supply operation. A resistance of 50 Ω was chosen to make the drain current 20 mA. The drain-bias circuit is included in the output matching circuit. The bypass capacitor C_D and dc-block capacitor C_c have a capacitance of 12 pF and 8 pF, respectively.

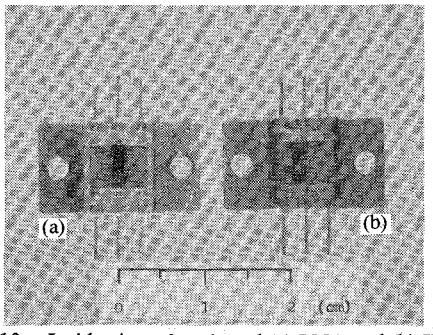

Fig. 13. Inside view of packaged (a) LNA and (b) IFA.

III. Device Packaging

For evaluation of the LNA and IFA MMIC's in a DBS receiver, a specially designed universal hermetic package has been provided. It is a rectangular stripline package with a copper flange. The packaged LNA and IFA are shown in Fig. 13 (a) and (b), respectively, with top covers removed. The LNA contains a three-stage LNA chip. The IFA contains two cascaded three-stage IFA chips. The two center leads are for RF input and output. While other leads can be used for dc biasing, only one of them is employed in the present application since the MMIC chips are designed for single power supply operation. The dc-bias connection to the chips is done via a dielectric standoff. The DRO chip has been mounted together with a dielectric resonator in a hermetically sealed MIC housing with outer dimensions of 25×25×12 mm.

IV. Device Fabrication

The LNA chip was fabricated using an epitaxial wafer with active and buffer layers successively grown on Cr-doped semi-insulating substrate by a metal-organic chemical vapor deposition method. The carrier concentration and thickness of the active layer are 2.0×10^{17} cm^{-3} and 0.5 μm, respectively. Mesas are formed to define FET active areas and resistors.

The IFA and the DRO MMIC's were fabricated by selective Si ion implantation into undoped semi-insulating GaAs substrates. A resist/SiO_2 film is used as a mask for the ion implantation. The acceleration energy and dose are 70 keV and 3.5×10^{12} cm^{-2} for FET active layers. For FET contact layers and resistor layers, Si ions are dually implanted at a dose of 2×10^{13} cm^{-2} and energies of 250 and 120 keV. After ion implantation and removal of the resist/SiO_2 film, the wafers are annealed at 850°C for 15 min in AsH_3/Ar atmosphere without encapsulants.

The gates of the FET's in the LNA are defined to a length 0.4 μm by using electron-beam lithography. The gate is recessed in order to attain a low noise figure. The gate length of FET's in the IFA and DRO MMIC's is 1 μm, and the widths are 600 and 300 μm, respectively. They were delineated by conventional photolithography.

The Schottky-barrier gate electrodes are formed of Al with a thickness of 6000 Å. The ohmic electrodes are formed by alloying Pt/AuGe at 450°C. The first-level metallization of the MIM capacitor is a 0.8-μm-thick Al.

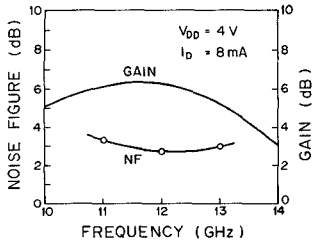

Fig. 14. Measured noise figure and gain of a single-stage low-noise amplifier as a function of frequency.

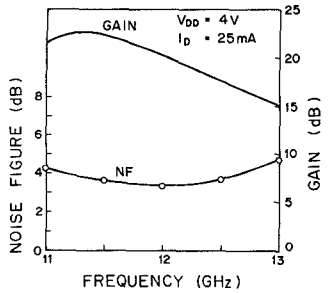

Fig. 15. Measured noise figure and gain of a three-stage low-noise amplifier as a function of frequency.

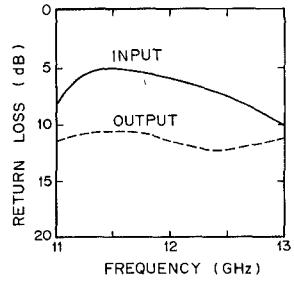

Fig. 16. Measured input and output return loss of a three-stage low-noise amplifier as a function of frequency.

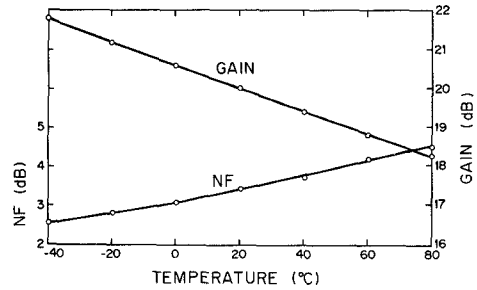

Fig. 17. Temperature dependence of noise figure and gain of a three-stage LNA.

$CVD\ SiO_2$ film with a thickness of 3,500 Å is used as the capacitor dielectric. The Au/Pt/Ti metal systems are used for the top plates of the capacitors, the bonding pad, and the interconnection metals. All of the metal patterns are formed by a liftoff process.

The MMIC chips are all glassivated with a CVD SiO_2 film, except for the bonding area. After lapping the substrate to a thickness of 300 μm, the backside of the wafer is metallized.

V. RF Performance

A. Low-Noise Amplifier

Fig. 14 shows the measured frequency response of the noise figure and gain of the single-stage LNA at a drain voltage $V_{DD} = 4$ V and a drain current $I_D = 8$ mA. The MMIC chip is mounted on a coplanar test fixture. A minimum noise figure of 2.8 dB and a gain of 6.5 dB are obtained at 12 GHz, including the test fixture loss of 0.3 dB. The discrepancy between predicted and measured noise figures is mainly due to the performance variation of the FET employed in the MMIC.

The three-stage LNA chip was evaluated after mounting into the hermetic ceramic package as shown in Fig. 13 (a). Fig. 15 shows the measured frequency response of the noise figure and gain of the LNA operated at $V_{DD} = 4$ V and a total current $I_D = 25$ mA. A minimum noise figure of 3.4 dB and a gain of 20 dB were obtained at 12 GHz, and a noise figure ≤ 3.4 dB and a gain ≥ 19.5 dB were obtained at frequencies from 11.7–12.2 GHz. These measured results also include the test fixture loss of 0.4 dB.

The minimum noise figure and the gain are in good agreement with the values predicted from the single-stage LNA performance. The frequency of maximum gain, however, is shifted towards a lower frequency. This might be caused by an interstage matching problem.

Fig. 16 shows the measured frequency response of input and output return losses of the three-stage LNA. An input return loss ≥ 6 dB (VSWR ≤ 3.0) and an output return loss ≥ 12 dB (VSWR ≤ 1.7) were obtained at frequencies from 11.7–12.2 GHz. The input VSWR characteristic is similar to that of the single-stage LNA, measured using the coplanar test fixture. However, the output VSWR is worse than that of the single-stage LNA. The disagreement is due to the dimensional limitation of the ceramic package. The inner dimension of the package is about one and half times longer than the MMIC chip length. Since the MMIC chip has been mounted at the input terminal side of the package, long bonding wires are used to connect the output pad of the chip and output terminal of the package. The bonding wire has an inductance of ~ 1.0 nH, causing the output VSWR discrepancy between the measurement and design.

Fig. 17 shows the temperature dependence of the noise figure and the gain for the packaged three-stage LNA at 12 GHz. The noise figure of ≤ 4.4 dB and the gain of ≥ 18.4 dB were obtained over the temperature range of -40–$80\,^{\circ}$C.

B. IF Amplifier

The three-stage IFA chip was also evaluated after mounting in the hermetic ceramic package. Fig. 18 shows the measured frequency response of the noise figure and gain of the IFA operated at a drain voltage $V_{DD} = 7$ V and a total current $I_D = 39$ mA. A noise figure ≤ 3.9 dB and a gain 23.5 ± 0.1 dB were obtained from 0.5–1.5 GHz. The measured gain performance shows good agreement with the simulated result. However, the noise figure is somewhat

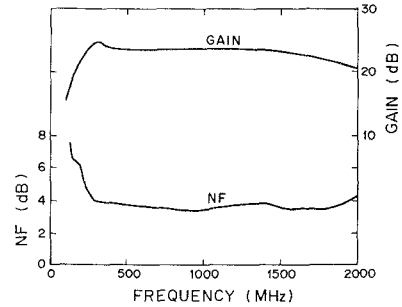

Fig. 18. Measured noise figure and gain of a 1-GHz IF amplifier as a function of frequency.

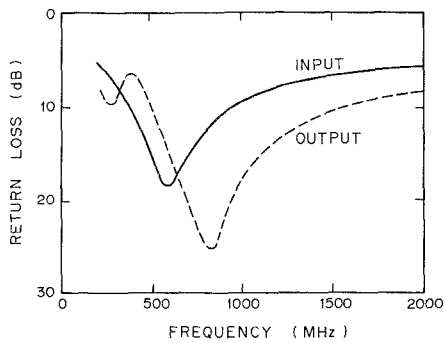

Fig 19. Measured input and output return loss of a 1-GHz IF amplifier as a function of frequency.

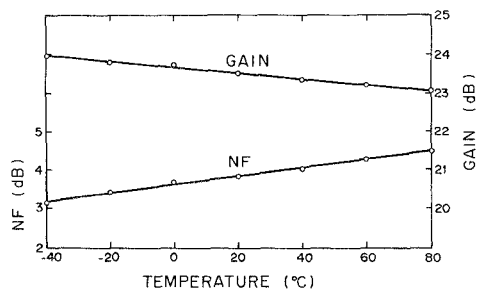

Fig. 20. Temperature dependence of the noise figure and gain of IFA

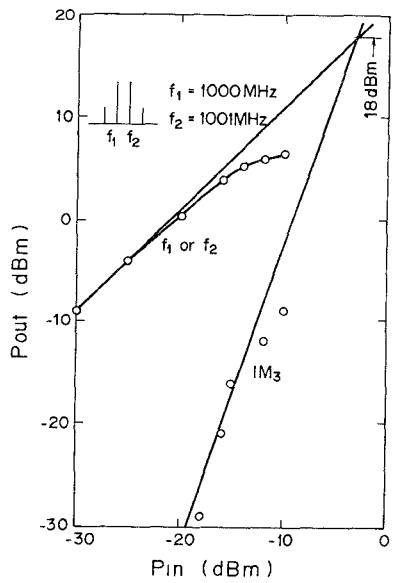

Fig. 21. Third-order intermoduration products of IFA.

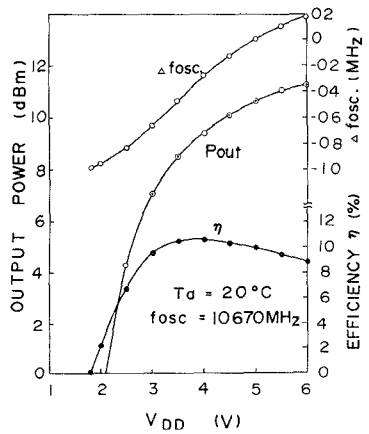

Fig 22. Measured output power (P_{out}), oscillation frequency deviation (Δf_{osc}), and efficiency (η) of a dielectric resonator oscillator as a function of drain voltage (V_{DD}).

poorer than the predicted performance. This may be due to insufficient noise modeling of the FET's, whose noise parameters were obtained by simple scaling from the measured ones of the 300-μm gate width FET.

Fig. 19 shows the measured frequency response of input and output return loss. An input return loss ≥ 7 dB (VSWR ≤ 2.6) and an output return loss ≥ 11 dB (VSWR ≤ 1.8) were attained in the same frequency band. Although the IFA has been designed to minimize the input and output VSWR's at a center frequency of 1 GHz, the measured minimum input and output VSWR's are shifted towards lower frequencies. A computer simulation can explain this discrepancy if we assume that the gate–source capacitance of the FET is larger, by a factor 1.3, than that used in the design.

Fig. 20 shows the temperature dependence of the noise figure and the gain for the IFA at 1 GHz. A noise figure of ≤ 4.5 dB and a gain of ≥ 23 dB were obtained over the temperature range of -40–$80\,^{\circ}$C. No major changes are observed for gain flatness or input and output VSWR's. Fig. 21 shows the third-order intermodulation products of the IFA. It is found that the output power at the 1-dB gain compression point and the third-order intercept point are measured to be 8 and 18 dBm, respectively.

Since an IF amplifier gain of ≥ 40 dB was required to operate the outdoor unit, two IFA chips were cascaded in the package as shown in Fig. 13 (b). The measured gain of the cascaded IF amplifier was 45 ± 0.3 dB over 0.5–1.5 GHz, and the input and output VSWR's are similar to those of the single-chip IFA.

C. Dielectric Resonator Oscillator

Fig. 22 shows the measured drain voltage V_{DD} dependence of output power P_{out}, oscillation frequency deviation Δf, and efficiency (η) of the DRO with a center oscillation frequency of 10.67 GHz. An output power of 10.5 dBm with 10-percent efficiency was obtained at a drain voltage $V_{DD} = 5$ V. The frequency pushing is ~ 0.2 MHz/V. Since

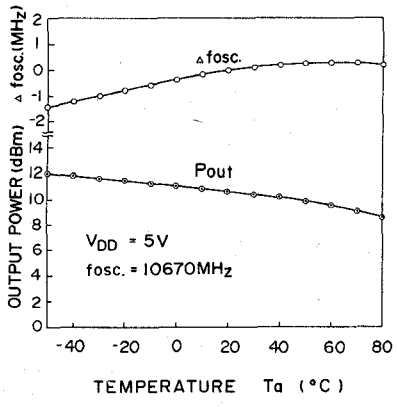

Fig. 23. Measured temperature dependence of the oscillation frequency deviation (Δf_{osc}) and output power (P_{out}) of a dielectric resonator oscillator.

the measured frequency pulling for VSWR = 1.5 is ~ 400 kHz, the external Q of the DRO is calculated to be ~ 10 000.

Fig. 23 shows the temperature dependence of frequency deviation (Δf) and the output power (P_{out}). It is found that the frequency variation is 1.5 MHz (1.2 ppm/°C) and the output power variation is 4 dB over a temperature range from −40–80°C.

VI. DBS Receiver Application

An outdoor unit of a DBS receiver has been modified to accommodate the developed LNA, IFA, and DRO MMIC's. The packaged LNA containing a three-stage chip and the packaged IFA containing two cascaded three-stage chips have been employed. The outdoor unit has exhibited an overall noise figure of $\leqslant 4$ dB for frequencies from 11.7–12.2 GHz.

VII. Conclusion

Three kinds of GaAs MMIC's have been developed for the DBS receiver. The low-noise amplifier has a noise figure of 3.4 dB and a gain of 19.5 dB for frequencies from 11.7–12.2 GHz. The IF amplifier has a noise figure of 3.9 dB and a gain of 22 dB for frequencies from 0.5–1.5 GHz. The DRO incorporating an MMIC chip and a dielectric resonator gives an output power of 10 mW at 10.67 GHz and a frequency stability of 1.5 MHz over the temperature range of −40–80°C. All MMIC chips incorporate self-biasing source resistors and bypass capacitors for single power supply operation, and are contained in hermetic ceramic packages or housings. The DBS receiver using three MMIC chips exhibits an overall noise figure of $\leqslant 4.0$ dB for frequencies from 11.7–12.2 GHz.

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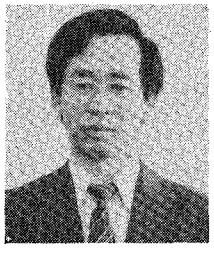


Shigekazu Hori was born in Wakayama, Japan, on January 2, 1946. He received the B.S. and M.S. degrees from Tokyo Institute of Technology, Tokyo, Japan, in 1969 and 1971, respectively.

In 1971, he joined the Toshiba Corporation in Kawasaki, Japan. Since then, he has been engaged in the development of MIC modules for radar and communications systems. Recently, he has been working on the development of low-noise and high-power GaAs FET amplifiers using MIC and MMIC technology.

Mr. Hori is a member of the IECE of Japan.

Kiyoho Kamei was born in Aichi, Japan on May 18, 1944. He received the B.S. and M.S. degrees in electronic engineering from Nagoya University, Japan, in 1967 and 1969, respectively.

He joined Toshiba Corporation, Kawasaki, Japan, in 1969, where he has been engaged in the research and development of GaAs devices.

Mr. Kamei is a member of the Japan Society of Applied Physics.

Kiyoyasu Shibata was born in Tokyo, Japan on December 6, 1950. He received the B.S. and M.S. degrees in electronics engineering from the Tokyo Institute of Technology, Japan, in 1973 and 1975, respectively.

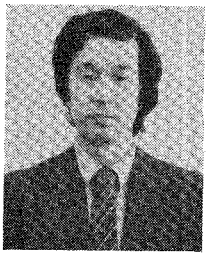
In 1975, he joined the Toshiba Corporation in Kawasaki, Japan. Since then, he has been engaged in the evaluation of GaAs FET's and development of GaAs FET amplifiers. Recently, he has been working on the development of GaAs MMIC's.

Mr. Shibata is a member of the IECE of Japan.

Katsuhiko Mishima was born in Hiroshima, Japan, on July 5, 1942. He received the B.S. and M.S degrees in electronic engineering from Tokyo University, Tokyo, Japan, in 1965 and 1967, respectively.

From 1967 to 1979, he was with the Research and Development Center of the Toshiba Corporation, Kawasaki, Japan. Since 1979, he has been with the Electronic Equipment Division of the company. His research and development work has concentrated on circuit applications of microwave semiconductor devices and monolithic microwave integrated circuits.

Mr. Mishima is a member of the IECE of Japan.



Mikio Tatematsu was born in Nagoya, Japan, on January 18, 1952. He received the B.S. and M.S. degrees in Physics from Nagoya University, Nagoya, in 1975 and 1977, respectively.

He joined the Toshiba Corporation, Kawasaki, Japan, in 1977, where he has been engaged in the research and development of GaAs IC's and other devices.

Susumu Okano was born in Tokyo, Japan, on February 5, 1942. He received the B.S. and M.S. degrees in electronic engineering from Tokyo University, Tokyo, Japan, in 1964 and 1966, respectively.

Since joining the Toshiba Corporation in 1966, he has worked on Si and GaAs microwave semiconductor devices. At present, he is Manager of the Semiconductor Devices Group and also Head of the GaAs MMIC development team in the Microwave Solid-State Department.